CLAIMS

1. A microcontroller device, comprising:

a control unit, the control unit having a plurality of logic modules including a processing module for executing processing procedures; an interrupt managing module for managing program interruptions caused by internal or external events; and an arbiter module for managing switching of said plurality of modules; and

a set of interruption registers associated with said control unit for storing information regarding interrupts and for requesting arrest of said processing module for executing processing procedures.

2. The microcontroller device of claim 1, wherein said set of interruption registers comprises:

a register of the served interrupts;

a register containing the information regarding which interrupt has interrupted execution of the processing procedure; and

a register in which there is stored the state of the module for managing the processing procedure at which said interrupt has occurred.

3. The microcontroller device of claim 2, wherein the control unit writes said information directly in said interrupt registers and sends a selection signal containing an information on the interrupt served.

4. The microcontroller device of claim 3, wherein downstream of the register of the served interrupts and of the register containing the information regarding which interrupt has interrupted execution of the processing procedure, there are provided respective multiplexers driven by said selection signal, and in that the outputs of said multiplexers are sent at input to a logic gate to obtain a return selection signal.

5. The microcontroller device of claim 1, wherein said plurality of logic modules comprises finite state machines.

6. The microcontroller device of claim 1, wherein said processing module is configured for executing iterative processing procedures.

7. A method for managing the program interrupts in a microcontroller device, which provides for the using of a module for managing the executive processing procedure of a control unit belonging to said microcontroller device for executing processing procedures and provides for managing interrupts by means of an interrupt managing module, the method comprising the following operations:

upon occurrence of an interrupt in a state of the processing procedure, transferring the control from the module for managing the executive processing procedure to the interrupt managing module;

storing the information regarding the interrupt that has occurred in interrupt registers;

at the end of the interrupt, transferring control to the interrupt managing module for execution of an instruction of a "return from interrupt" type; and

restoring the control to the module for managing the processing procedure at the state in which the interrupt occurred.

8. The method of claim 7, including the operations of:

evaluating whether the interrupt has occurred at a standard instruction; and

in the negative, restoring the control to the module for managing the processing procedure at the state where the interruption occurred; and

in the positive, restoring the control to an arbiter module.

9. The method of claim 8, wherein said operations of restoring the control to an arbiter module take place under the control of a return selection signal obtained from the information regarding the interrupt that has occurred stored in the interrupt registers.

10. The method of claim 7, wherein the information regarding the interrupt that has occurred and which is stored in the interrupt registers comprises information regarding the interrupt served, information regarding the interrupt that has occurred during the processing procedure, and the state of the processing procedure in which the interrupt that has occurred.

11. The method of claim 7, comprising the operation of configuring said processing module for execution of iterative processing procedures.

12. A computer program product directly loadable in the memory of a computer and comprising software code portions that perform the method of claim 7.

13. A microcontroller device, comprising:

a control unit comprising a processing module and an interrupt managing module;

a first register having an input coupled to the control unit, the first register configured to store interrupts;

a second register having an input coupled to the control unit and configured to store information regarding an interrupt that has interrupted execution of a processing procedure;

a third register having an input coupled to the control unit configured to store the state of the processing module at the time the interrupt occurs; and and

a logic gate having a first input coupled to the first register and a second input coupled to the second register and an output coupled to the control module.

14. The device of claim 13, further comprising a first multiplexer coupled between the first register and the first input of the logic gate and a second multiplexer coupled between the second register and the second input of the logic gate, the first and second multiplexers each having an input coupled to a selection signal output of the control unit.

15. The device of claim 14, wherein the processing module is configured to execute processing procedures, and the interrupt managing module is configured to manage program interruptions caused by internal and external events; and wherein the control unit further comprises an arbiter module for managing switching of the processing module and the interrupt managing module.

16. The device of claim 15, wherein the control unit is configured to write information directly in the first, second, and third registers.

17. The device of claim 16, wherein the processing module, the interrupt managing module, and the arbiter module each comprise finite state machines.

18. A method for managing program interrupts in a microcontroller device having a control unit that includes a processing module, an interrupt managing module, and an arbiter module, the device further including a set of interruption registers for storing information regarding interrupts and for requesting arrest of the processing module for executing processing procedures, the control unit configured to write information directly to the interrupt registers and to send a selection signal containing information regarding an interrupt, the method comprising:

receiving an interrupt in the control unit;

upon receipt of the interrupt, transferring control from the processing module to the interrupt managing module;

storing information regarding the interrupt into the set of interruption registers;

processing the interrupt; and

transferring control of the interrupt managing module at the end of the interrupt to the processing module at the state at which the interrupt occurred.

19. The method of claim 18, wherein receiving the interrupt comprises evaluating whether the interrupt has occurred at a standard instruction, and in the negative restoring the control to the processing module at the state where the interrupt occurred, and in the negative restoring control to the arbiter module.

20. The method of claim 19, wherein transferring control to the arbiter module comprises generating a return selection signal in response to information stored in the set of interrupt registers.

21. A microcontroller device, comprising:

a control unit that comprises a processing module for executing processing procedures having an output, an interrupt managing module having an input coupled to the output of the processing module, the interrupt managing module configured to manage program interruptions caused by one of at least internal and external events;

a loading manager module for managing loading of data into the control unit, and an arithmetic-operations manager module for managing arithmetic operations, the arbiter module configured to execute the operation of downloading instructions from a memory;

a first register having an input coupled to an output of the control unit, the first register configured to store interrupts;

a first multiplexer coupled to an output of the first register and having an output, the first multiplexer further having a control terminal coupled to a control output of the control unit;

a second register having an input coupled to an output of the control unit, the second register configured to store information regarding an interrupt that has interrupted execution of a processing procedure managed by the processing module;

a second multiplexer coupled to the second register and having an output, the second multiplexer further including a control terminal coupled to the control signal output of the control unit;

a third register having an input coupled to an output of the control unit, the third register configured to store the state of the processing module at the time the interrupt occurs; and

a logic gate having a first input coupled to the output of the first multiplexer, a second input coupled to the output of the second multiplexer, and an output coupled to an input of the control unit, the logic gate configured to generate a return selection signal, the processing module configured to transfer control to the interrupt managing module upon receipt of an interrupt signal, the control unit configured to write information directly to the first, second, and third registers regarding the interrupt, and upon receipt of a predetermined return selection signal, to transfer control to the interrupt managing module for execution of an instruction of a return-from-interrupt type that restores control to the processing module at the state at which the processing module was in at the time the interrupt occurred.